R20 Regulation *Subject code: 3E5DA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech V Semester Supplementary Examinations, April 2026

DIGITAL DESIGN THROUGH VERILOG HDL

(ECE)

Maximum Marks: 70 Date: 27.04.2026 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		Marks	CO	BTL
1	Write the differences between simulation and synthesis.	2M	1	L1
2	Mention data types used in Verilog HDL.	2M	1	L1
3	Write with an example Array of Instances of Primitives.	2M	2	L1
4	Define net delay with an example.	2M	2	L1
5	Write about Bitwise operators in Verilog.	2M	3	L1
6	Write about bidirectional gates.	2M	3	L1
7	Write the syntax of even construct.	2M	4	L1
8	Write a Verilog module for 2 to 4 decoder using case statement.	2M	4	L1
9	Write about $display task.	2M	5	L1
10	Write a simple UDP table for 2 input AND gate.	2M	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
11	Discuss the various modeling styles available in Verilog HDL.	10M	1	L2
	OR			
12	Explain parameter declaration and assignments with example.	10M	1	L2
13	Design full subtractor using basic logic primitives.	10M	2	L2
	OR			
14	Write a Verilog code for 2 input Nand gate and its test bench code.	10M	2	L2
15	Explain about operators in Verilog with examples.	10M	3	L2
	OR			
16	Write a Verilog code & its test bench for a 4-bit comparator with all expected input/output wave forms.	10M	3	L2
17	Explain blocking and Non-blocking statements with examples.	10M	4	L2
	OR			
18	Design 4:1 multiplexer in behavioral modeling style.	10M	4	L2
19	Briefly explain combinational UDPs in Verilog.	10M	5	L2
	OR			
20	Analyze the processes involved in file-based tasks and functions.	10M	5	L2